64. (New) An image display device comprising: a plurality of pixels arranged in the shape of a matrix such that the pixels are surrounded with a plurality of data signal lines arranged in a direction of column and a plurality of scanning signal lines arranged in a direction of row; a data signal line drive circuit for supplying a video signal to the data signal lines; and a scanning signal line drive circuit for supplying a scanning signal to the scanning signal lines, wherein

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the logical circuit as claimed in claim 37 is used as at least one part of a logical circuit receiving an output pulse of a shift register circuit constituting the scanning signal line drive circuit and one of a plurality of control signals inputted from outside as input signals and outputting signals simultaneously to a plurality of shift register circuits having a different combination.

Please **cancel** claims 4-17, 22-36, and 54-57 without prejudice.

REMARKS

The following is in response to the Office Action mailed December 26, 2002, in the above-referenced application.

Claims 1-3, 18-21, 37-53, and 58-64 are pending in the subject application. Claims 1, 18, and 37 have been amended, and new claims 61-64 have been added by the present amendment. Claims 4-17, 22-36, and 54-57 have been canceled without prejudice. The amendments are fully supported by the specification as originally filed.

Applicants have amended the specification to make specific reference to the parent application (U.S. Serial No. 09/300,178, filed on April 27, 1999), thereby perfecting the right of priority under 35 USC 120. It is noted that Applicants previously submitted certified copies of the following Japanese applications: 10-117955, 10-364774, and 11-105236. Certified copies of these applications were filed in the parent

application (U.S. Serial No. 09/300,178); therefore it is unnecessary to resubmit the certified copies (see MPEP 201.14(b)).

In response to the objections to the specification, claims 54-57 have been canceled and replaced with corresponding claims 61-64, which are reordered so that claim 58 is not separated from claim 53, and new claim 62 (same as canceled claim 57) is not separated from new claim 61 (same as canceled claim 54). The specification also has been amended to eliminate references to particular claims. Withdrawal of the objections is respectfully requested.

Claims 1-19 and 38-41 were rejected under 35 USC 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter of the invention. These rejections are respectfully traversed in view of at least the amendments and arguments contained herein.

With reference to independent claims 1 and 18, Applicants claim a latch circuit and a shift register circuit made up of a plurality of latch circuits, respectively, wherein each latch circuit includes: a first input of a pulse signal, a second input of a clock signal, and an output comprising the pulse signal in synchronization with the clock signal such that an amplitude of the clock signal is smaller than an amplitude of the pulse signal.

The Applicant's invention is exemplified by the latch circuit diagram of FIG. 3. As shown in FIG. 3, latch circuit LAT includes clock signal input control sections 12 and 13 for inputting a clock signal ck (/ck) and a pulse signal in (/in), where the clock signal has an amplitude smaller than an amplitude of the pulse signal. For example, in the embodiment of FIGS. 1-4, the clock signal is 5 V and the pulse signal is 16 V.

The above-described latch circuit can yield significant benefits. By inputting clock signals having a voltage lower than the pulse voltage of the circuit, the consumption of power by the clock signals is reduced. Moreover, in a shift register

circuit constructed by serially connecting a plurality of latch circuits, power consumption is reduced in the shift register circuit and, therefore, the liquid crystal device can operate at a reduced level of power.

In response to the rejections under 35 USC 112, second paragraph, claims 1 and 18 have been amended to eliminate any indefinite language. For example, claim 1 recites a first input comprising the pulse signal and a second input comprising the clock signal, such that the amplitude of the clock signal is smaller than the amplitude of the pulse signal. Claim 18 has been similarly amended, wherein the shift register circuit includes a plurality of latch circuits, each of the latch circuits receiving a clock signal and a pulse signal as inputs, the amplitude of the clock signal being smaller than the amplitude of the pulse signal. Therefore, it is believed that claims 1-19 overcome the rejections under 35 USC 112, second paragraph.

With reference to independent claim 37, Applicants claim a CMOS logical circuit, including: a first input signal having a first amplitude and a second input signal having a second amplitude, wherein the amplitude of at least one of the input signals is smaller than a drive voltage of the CMOS logical circuit.

The Applicants' invention as recited in claim 37 is exemplified by FIG. 51, which depicts "first" input signals IN1 and /IN1 having an amplitude of 5 V, and "second" input signals IN2 and /IN2 having an amplitude of 15V. In FIG. 51, the amplitude of input signals IN1 and /IN1 is smaller than the drive voltage Vcc (15 V). Consequently, claim 37, as amended, clearly recites first and second input signals, as discussed in the specification. It is respectfully requested that the rejections under 35 USC 112, second paragraph, be withdrawn.

It is believed the application is in condition for immediate allowance, which action is earnestly solicited.

The Applicants believe that additional fees are not required for consideration of the within Amendment. However, if for any reason a fee is required, a fee paid is inadequate or credit is owed for any excess fee paid, you are hereby authorized and requested to charge Deposit Account No. **04-1105**.

Respectfully submitted,
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APPENDIX A:
VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION

The following has been added to page 1, after the title:

CROSS-REFERENCE TO RELATED APPLICATION(S)

This application is a continuation-in-part of copending application U.S. Serial No. 09/300,178, filed on April 27, 1999.

The paragraph on page 83, line 24 to page 84, line 15 has been amended as follows:

Fig. 1 is a block diagram showing an example of [the] a shift register circuit [mentioned in claim 14] according to the present invention. This shift register circuit 11 is constructed by serially connecting a plurality of latch circuits (half latch circuits) LAT. That is, a start signal (pulse signal) st is inputted to the input node of the latch circuit LAT of the first stage, while the input node of the latch circuit LAT of the second stage is connected to the output node. Likewise, the input node of each latch circuit LAT is connected to the output node of the preceding stage, while the output node is connected to the input node of the latch circuit LAT of the succeeding stage. Then, a clock signal ck is inputted to the control nodes of the latch circuits LAT of the odd-number stages. In contrast to this, a clock signal /ck that is the inverted signal of the clock signal ck is inputted to the control nodes of the latch circuits LAT of the even-number stages.

The paragraph on page 85, lines 3-12 has been amended as follows:

Fig. 2 shows a circuit diagram showing an example of the construction of [the] a latch circuit [mentioned in claim 4] that constitutes the shift register circuit 11 of Fig. 1. To the source electrodes of two p-type transistors M11 and M12 that serve as first and second p-type transistors is connected a power potential Vcc (=16 V). Then, the gate

electrode of the p-type transistor M11 is connected to the drain electrode of the p-type transistor M12, while the gate electrode of the p-type transistor M12 is connected to the drain electrode of the p-type transistor M11.

The paragraph on page 86, lines 20-24 has been amended as follows:

Fig. 3 shows a latch circuit LAT that serves as an example of [the] a shift register circuit [mentioned in claim 18] constructed by incorporating the first and second clock signal input sections 12 and 13 to the latch circuit of Fig. 2.

The paragraph on page 92, lines 16-17 has been amended as follows:

Fig. 5 shows [an] another example of [the] a latch circuit [mentioned in claim 5] according to the present invention.

The paragraph on page 95, lines 19-20 has been amended as follows:

Fig. 7 shows [an] another example of [the] a latch circuit [mentioned in claim 7] according to the present invention.

The paragraph on page 96, lines 9-10 has been amended as follows:

Fig. 8 shows [an] another example of [the] a latch circuit [mentioned in claim 8] according to the present invention.

The paragraph on page 97, lines 10-13 has been amended as follows:

Fig. 9 shows an example of [the] a latch circuit [mentioned in claim 9] constituting the logical product and non-disjunction circuits AND-NOR1 and AND-NOR2 shown in Fig. 8.

The paragraph on page 98, lines 6-7 has been amended as follows:

Fig. 10 shows [an] another example of [the] a latch circuit [mentioned in claim 10] according to the present invention.

The paragraph on page 99, lines 4-6 has been amended as follows:

Fig. 11 shows an example of [the] a latch circuit [mentioned in claim 11] constituting the first and second non-conjunction circuits NAND1 and NAND2 shown in Fig. 10.

The paragraph on page 99, lines 18-19 has been amended as follows:

Fig. 12 shows [an] another example of [the] a latch circuit [mentioned in claim 12] according to the present invention.

The paragraph on page 100, lines 6-7 has been amended as follows:

Fig. 13 shows [an] another example of [the] a latch circuit [mentioned in claim 13] according to the present invention.

The paragraph on page 101, lines 12-13 has been amended as follows:

Fig. 15 shows [an] another example of [the] a latch circuit [mentioned in claim 12] according to the present invention.

The paragraph on page 102, lines 17-18 has been amended as follows:

Fig. 16 shows [an] another example of [the] a latch circuit [mentioned in claim 13] according to the present invention.

The paragraph on page 103, lines 12-13 has been amended as follows:

Fig. 17 shows [an] another example of [the] a latch circuit [mentioned in claim 14] according to the present invention.

The paragraph on page 104, lines 22-23 has been amended as follows:

Fig. 18 shows [an] another example of [the] a latch circuit [mentioned in claim 15] according to the present invention.

The paragraph on page 106, lines 5-7 has been amended as follows:

Fig. 19 shows an example of the first clock signal input control section 12 of [the] a shift register [mentioned in claims 24 through 26] according to the present invention.

IN THE CLAIMS

Claims 1, 18, and 37 have been amended as follows:

1. (Amended) A latch circuit [which receives] for synchronizing a pulse signal [and] with a clock signal [as inputs and], comprising:

a first input comprising the pulse signal;

a second input comprising the clock signal; and

[transmits] an output comprising the pulse signal in synchronization with the clock signal, wherein the clock signal [or the pulse signal having] has an amplitude smaller than an amplitude of the pulse signal outputted from the latch circuit.

18. (Amended) A shift register circuit having a plurality of latch circuits for transmitting a pulse signal in synchronization with a clock signal, each of the latch circuits comprising:

[the latch circuits each internally having] a clock signal input control section for executing control to input and stop the supplied clock signal, [and] wherein the clock

signal [having] has an amplitude smaller than [the] an amplitude of the pulse signal; and

an output comprising the pulse signal in synchronization with the clock signal.

37. (Amended) A CMOS logical circuit [consisting of Complementary Metal-Oxide Semiconductors] which performs a logical operation based on a plurality of input signals, the CMOS logical circuit comprising:

a first input signal having a first amplitude; and

a second input signal having a second amplitude;

[an] wherein the amplitude of at least one of the input signals is smaller than a drive voltage of the CMOS logical circuit.

The following new claims have been added:

61. (New) An image display device comprising: a plurality of pixels arranged in the shape of a matrix such that the pixels are surrounded with a plurality of data signal lines arranged in a direction of column and a plurality of scanning signal lines arranged in a direction of row; a data signal line drive circuit for supplying a video signal to the data signal lines; and a scanning signal line drive circuit for supplying a scanning signal to the scanning signal lines, wherein

the logical circuit as claimed in claim 37 is used as a logical circuit receiving an output pulse of a shift register circuit constituting the data signal line drive circuit and a pulse width control signal inputted from outside as input signals and generating an output signal having a pulse width smaller than the pulse width of the output pulse of the shift register circuit.

62. (New) An image display device as claimed in claim 61, wherein in the logical circuit constituting the data signal line drive circuit and the scanning signal line drive circuit, an output signal of the shift register circuit is inputted to a gate electrode of the transfer transistor.

63. (New) An image display device comprising: a plurality of pixels arranged in the shape of a matrix such that the pixels are surrounded with a plurality of data signal lines arranged in a direction of column and a plurality of scanning signal lines arranged in a direction of row; a data signal line drive circuit for supplying a video signal to the data signal lines; and a scanning signal line drive circuit for supplying a scanning signal to the scanning signal lines, wherein

the logical circuit as claimed in claim 37 is used as a logical circuit receiving an output pulse of a shift register circuit constituting the scanning signal line drive circuit and a pulse width control signal inputted from outside as input signals and generating an output signal having a pulse width smaller than the pulse width of the output pulse of the shift register circuit.

64. (New) An image display device comprising: a plurality of pixels arranged in the shape of a matrix such that the pixels are surrounded with a plurality of data signal lines arranged in a direction of column and a plurality of scanning signal lines arranged in a direction of row; a data signal line drive circuit for supplying a video signal to the data signal lines; and a scanning signal line drive circuit for supplying a scanning signal to the scanning signal lines, wherein

the logical circuit as claimed in claim 37 is used as at least one part of a logical circuit receiving an output pulse of a shift register circuit constituting the scanning signal line drive circuit and one of a plurality of control signals inputted from outside as input signals and outputting signals simultaneously to a plurality of shift register circuits having a different combination.

Claims 4-17, 22-36, and 54-57 have been canceled without prejudice.